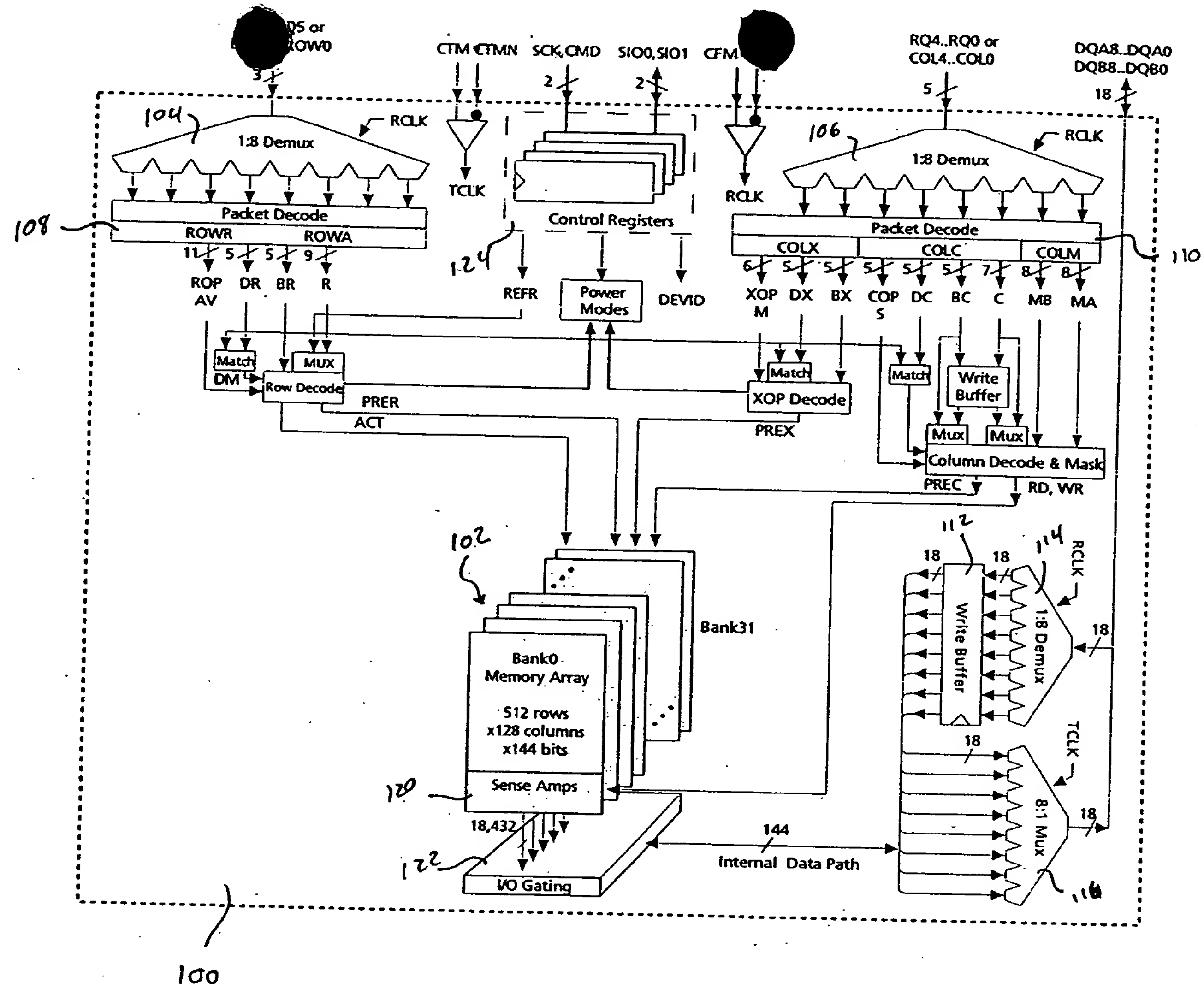
CTM CTMN
SCK,CMD
SIO0,SIO1
CFM
RQ4..RQ0 or
COL4..COL0
DQA8..DQA0
DQB8..DQB0
104
1:8 Demux
RCLK
TCLK
Control Registers
106
1:8 Demux
RCLK
108
Packet Decode
ROWR
ROWA
ROP AV
DR
BR
R
124
REFR
Power Modes
DEVID
Packet Decode
COLX
COLC
COLM
110
XOP M
DX
BX
COP S
DC
BC
C
MB
MA
Match
MUX
DM
Row Decode
PRER
ACT
Match
XOP Decode
PREX
Match
Write Buffer
Mux
Mux
Column Decode & Mask
PREC
RD, WR
102
Bank31
Bank0
Memory Array
512 rows
x128 columns
x144 bits
Sense Amps
120
18,432
122
I/O Gating
144
Internal Data Path
112
114
RCLK
Write Buffer
1:8 Demux
TCLK
8:1 Mux
116
100

Fig. 1

150

(TOP VIEW)

10	VDD	GND		VDD	GND	VDD					VDD	VDD	VDD		GND	VDD
9																
8	VDD	CMD	VDD	GND	GNDa	GNDa	VDD	VDD	GND	GND	VDD	VDD	GND	GND	VCMOS	VDD
7	DQA8	DQA7	DQA5	DQA3	DQA1	CTMN	CTM	RQ7	RQ5	RQ3	RQ1	DQB1	DQB3	DQB5	DQB7	DQB8
6																
5																
4	GND	DQA6	DQA4	DQA2	DQA0	CFM	CFMN	RQ6	RQ4	RQ2	RQ0	DQB0	DQB2	DQB4	DQB6	GND
3	GND	SCK	VCMOS	GND	VDD	GND	VDDa	VREF	GND	VDD	GND	GND	VDD	SIO0	SIO1	GND
2																
1	VDD	GND		GND	VDD	GND					GND	GND	GND		GND	VDD
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	S

Fig. 2